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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

**Listing of Claims:** 

(Currently amended) A method of manufacturing a contact portion, the

method comprising:

forming a first signal line on a substrate;

forming an insulating layer covering on the first signal line and having a

contact hole exposing a surface of the first signal line;

forming a contact layer only on the exposed surface of the first signal line

through the contact hole  $\underline{by}$  soaking the substrate in chemical conversion solution

including a conductive material; and

forming a second signal line connected to the first signal line via the contact

layer,

wherein the first signal line is made of Al or Al alloy comprises one of Al and

Al alloy, and the second signal line is made of ITO or IZOcomprises one of indium

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tin oxide (ITO) and indium zinc oxide (IZO).

2. (Canceled)

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chemical conversion solution include-comprises at least one of W, Zr, Mo, and Cr.

(Currently amended) The method of claim 2claim 1, wherein the

4. (Currently amended) A method of manufacturing a thin film transistor

array panel, the method comprising:

forming a gate line on a substrate;

forming a gate insulating layer;

forming a semiconductor laver;

forming an ohmic contact layer;

forming a data line and a drain electrode;

forming a passivation layer having a first contact hole exposing the portion-a

portion of the drain electrode; and

forming a first contact layer only on the exposed surface-portion of the drain

electrode through the first contact hole by soaking the substrate in chemical

conversion solution including a conductive material.

5. (Canceled)

(Currently amended) The method of claim 5 claim 4, wherein the 6.

chemical conversion solution include comprises at least one of W, Zr, Mo, and Cr.

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7. (Currently amended) The method of claim 4, wherein the forming the

passivation layer comprises forming a second contact hole exposing the end portion

an end portion of one of the gate line or the data line and the data line is formed in the

step of forming the passivation layer.

8. (Currently amended) The method of claim 7, wherein-further

comprising forming a second contact layer is formed on the exposed surface end

portion of the one of the gate line or the data line and the data line through the second

contact hole in the step of forming, wherein the forming the second contact layer is

performed simultaneously with the forming the first contact layer.

(Currently amended) The method of claim 4, further comprising a step

of forming a storage electrode line-with the same layer as, wherein the forming the

storage electrode line is performed simultaneously with the forming the gate line.

10. (Currently amended) The method of claim 8claim 9, wherein a second

contact hole exposing the end portion an end portion of the storage electrode line is

formed in the step of forming the passivation layer.

11. (Currently amended) The method of claim 9claim 10, wherein further

 $\underline{comprising\ forming\ a\ second\ contact\ layer\ is\ formed\ on\ the\ exposed\ \underline{surface\ end}}$ 

portion of the storage electrode line through the second contact hole in the step of

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with the forming the first contact layer.

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forming, wherein the forming the second contact layer is performed simultaneously

12. (Currently amended) A contact portion comprising:

a substrate;

a first signal line formed on a substratethe substrate;

an insulating layer covering the first signal line and having a contact hole

exposing a surface of the first signal line;

a contact layer <u>disposed only</u> on the exposed surface of the first signal <u>line</u>

through the contact hole; and

a second signal line formed on the insulating layer and connected to the first

signal line via the contact layer,

wherein the first signal line is made of Al or Al alloycomprises one of Al and
Al alloy, and the second signal line is made of ITO or IZOcomprises one of indium

tin oxide (ITO) and indium zinc oxide (IZO).

13. (Currently amended) The contact portion of claim 12, wherein the

contact layer include comprises at least one of W, Zr, Mo, Cr, and an alloy including

at least one of W, Zr, Mo, and Cr.

14. (Original) The contact portion of claim 12, further comprising a lower

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layer formed under the first signal line.

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15. (Original) The contact portion of claim 14, wherein the lower layer is a

conductive layer including at least one of Cr, Ti, Mo, and MoW alloy.

16. (Currently amended) A thin film transistor array panel comprising:

a substrate:

a gate line formed on a substratethe substrate;

a gate insulating layer covering the gate line;

a semiconductor layer formed on the gate insulating layer:

a data line intersecting the gate line and having-comprising a source electrode,

the source electrode overlapping the portion of the semiconductor layer;

a drain electrode overlapping the portion of the semiconductor layer;

a passivation layer covering disposed on the data line and the drain electrode.

and having a first contact hole exposing the portion a portion of the drain electrode;

a first contact layer formed on the exposed surface of the drain electrode

through the first contact hole, and made of comprising a conductive oxide layer; and

a pixel electrode formed on the passivation layer and connected to the drain

electrode via the first contact laver.

17. (Original) The panel of claim 16, further comprising a color filter

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formed on the data line and the drain electrode.

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18. (Original) The panel of claim 16, further comprising a storage

electrode line formed with the same layer as the gate line.

19. (Original) The panel of claim 18, wherein the storage electrode line

includes Al and Al alloy.

20. (Currently amended) The panel of claim 18, wherein

the passivation layer and the gate insulating layer have a second contact hole

exposing the portion a portion of the storage electrode line, and

the panel further eomprising-comprises:

a second contact layer formed on the exposed portion on the storage electrode

line through the second contact hole; and

a contact assistant connected to the exposed portion of the storage electrode

line via the second contact layer.

21. (Currently amended) The panel of claim 20, wherein the second

contact layer include-comprises at least one of W, Zr, Mo, Cr, and an alloy including

W, Zr, Mo, Cr.

22. (Currently amended) The panel of claim 16, wherein

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one of the passivation layer or the and the gate insulating layer have a third

has a second contact hole exposing the portion a portion of one of the gate line or the

and the data line, and

the panel further comprising comprises:

a third second contact layer formed on the exposed portion on the gate line or

the data line through the third second contact hole; and

a contact assistant connected to the exposed portion of the one of the gate line

or the and the data line via the third second contact layer.

23. (Currently amended) The panel of claim 22, wherein the third second

contact layer include-comprises at least one of W, Zr, Mo, Cr, and an alloy including

W, Zr, Mo, Cr.

24. (Currently amended) The panel of claim 16, further comprising an

ohmic contact layer formed between the data line and the semiconductor layer and

between the drain electrode, and the and the semiconductor layer.

25. (Currently amended) The panel of claim 24, wherein the ohmic contact

layer has the same planar shape as the data line and the drain electrode, and the

semiconductor layer has the same planar shape as the data line and the drain electrode

except for the channel  $\underline{a}$  channel portion between the drain electrode and the source

electrode.

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26. (Currently amended) The panel of claim 16, wherein the first contact

layer include comprises at least one of W, Zr, Mo, Cr, and an alloy including W, Zr,

Mo. Cr.

27. (Original) The panel of claim 16, wherein the gate line includes a

conductive layer made of Al or Al alloy.

28. (Original) The panel of claim 16, wherein the data line includes a first

conductive layer made of Al or Al alloy.

29. (Currently amended) The panel of claim 28, wherein the data line

 $further\ comprise \underline{s}\ a\ second\ conductive\ layer\ formed\ under\ the\ first\ conductive\ layer.$ 

(Original) The panel of claim 29, wherein the second conductive layer

is made of a conductive layer including at least one of Cr, Ti, Mo, and MoW alloy.

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